CLAIMS

1. A nonvolatile floating gate memory cell comprising:

a semiconductor substrate;

a first doped region disposed in the semiconductor substrate;

a second doped region disposed in the semiconductor substrate and spaced apart from the first doped region, a channel region being defined in the semiconductor substrate between the first and second doped regions;

a floating gate disposed over a first part of the channel region and insulated therefrom by a first dielectric, the first dielectric being a tunnel dielectric and the floating gate having a top and a sidewall; and

a control gate having first and second sections respectively disposed upon the top and the sidewall of the floating gate, the second section of the control gate being insulated from the sidewall of the floating gate by a second dielectric, disposed over a second part of the channel adjacent the first doped region, and insulated from the second part of the channel by the first dielectric and the second dielectric.

2. The memory cell of claim 1 wherein the second section of the control gate is further disposed over at least part of the first doped region and is insulated therefrom by the first dielectric and the second dielectric.

3. The memory cell of claim 2 wherein the first section of the control gate is insulated from the top of the floating gate by the second dielectric.

4. The memory cell of claim 1 wherein:

the floating gate has an additional sidewall; and

the control gate further has a third section disposed upon the additional sidewall of the floating gate, and insulated therefrom by the second dielectric.

5. The memory cell of claim 4 wherein the floating gate is further disposed over at least part of the second doped region and insulated therefrom by the first dielectric.

6. The memory cell of claim 5 wherein:

the second section of the control gate is further disposed over at least part of the first doped region and is insulated therefrom by the first dielectric and the second dielectric; and

the third section of the control gate is further disposed over at least part of the second doped region and is insulated therefrom by the first dielectric and the second dielectric.

7. The memory cell of claim 6 wherein the first section of the control gate is insulated from the top of the floating gate by the second dielectric.

8. The memory cell of claim 4 wherein the third section of the control gate is disposed over a third part of the channel adjacent the second doped region and insulated from the third part of the channel by the first dielectric and the second dielectric.

9. The memory cell of claim 8 wherein:

the second section of the control gate is further disposed over at least part of the first doped region and is insulated therefrom by the first dielectric and the second dielectric; and

the third section of the control gate is further disposed over at least part of the second doped region and is insulated therefrom by the first dielectric and the second dielectric.

10. The memory cell of claim 9 wherein the first section of the control gate is insulated from the top of the floating gate by the second dielectric.

11. A nonvolatile floating gate memory cell comprising:

a semiconductor substrate;

a first doped region disposed in the semiconductor substrate;

a second doped region disposed in the semiconductor substrate and spaced apart from the first doped region, a channel region being defined in the semiconductor substrate between the first and second doped regions;

a floating gate disposed over a first part of the channel region and insulated therefrom by a tunnel dielectric, the floating gate having a top and first and second sidewalls on opposite sides thereof; and

a control gate having first, second and third sections respectively disposed upon the top, first sidewall, and the second sidewall of the floating gate, the second section of the control gate being disposed over a second part of the channel adjacent the first doped region, and the third section of the control gate being disposed over a third part of the channel adjacent the second doped region.

12. The memory cell of claim 11 wherein:

the control gate and the floating gate comprise polysilicon;

the first section of the control gate is separated from the top of the floating gate by an inter-poly dielectric;

the second section of the floating gate is separated from the first sidewall of the floating gate by the inter-poly dielectric, and is separated from the second part of the channel by the tunnel oxide and the inter-poly dielectric; and

the third section of the floating gate is separated from the second sidewall of the floating gate by the inter-poly dielectric, and is separated from the third part of the channel by the tunnel oxide and the inter-poly dielectric.

13. The memory cell of claim 11 wherein:

the control gate and the floating gate comprise polysilicon;

the first section of the control gate is separated from the top of the floating gate by an inter-poly dielectric;

the second section of the floating gate is separated from the first sidewall of the floating gate by the inter-poly dielectric, and is separated from the second part of the channel by the inter-poly dielectric; and

the third section of the floating gate is separated from the second sidewall of the floating gate by the inter-poly dielectric, and is separated from the third part of the channel by the inter-poly dielectric.

14. A method of forming a nonvolatile floating gate memory cell, comprising:

defining an active area in a semiconductor substrate;

forming a first dielectric over the active area, the first dielectric being a thin dielectric for allowing electron tunneling;

forming a strip of floating gate material over the first dielectric, the strip having a top and first and second sidewalls on opposite edges thereof;

forming a first spacer upon the first sidewall of the strip;

implanting a dopant into the semiconductor substrate aligned at least in part to the first spacer;

removing the first spacer;

forming a second dielectric over the strip and the substrate;

depositing a layer of control gate material over the second dielectric;

forming a word line mask over the control gate material; and

etching the control gate material layer, the second dielectric layer, and the strip through the word line mask to form a word line in self-alignment with the floating gate material and having a first control gate section along the first sidewall;

wherein at least part of the first control gate section and at least part of the floating gate overlay a channel region of the semiconductor substrate.

15. The method of claim 14 further comprising:

forming a second spacer upon the second sidewall of the strip;

implanting the dopant into the semiconductor substrate aligned at least in part to the second spacer; and

removing the second spacer prior to the second dielectric forming step;

wherein the word line of the etching step further has a second control gate section along the second sidewall; and

wherein at least part of the second control gate section overlays the channel region.

16. The method of claim 14 wherein the second dielectric forming step comprises depositing the second dielectric directly upon the first dielectric in proximity to the first sidewall.

17. A method of forming a nonvolatile floating gate memory cell, comprising:

defining an active area in a semiconductor substrate;

forming a first dielectric over the active area, the first dielectric being a thin dielectric for allowing electron tunneling;

forming a strip of floating gate material over the first dielectric, the strip having a top and first and second sidewalls on opposite edges thereof;

forming a first spacer of a predetermined thickness upon the first sidewall of the strip;

implanting a dopant into the semiconductor substrate aligned at least in part to the first spacer;

removing the first spacer;

forming a second dielectric of a predetermined thickness over the strip and the first dielectric in proximity to the first sidewall;

depositing a layer of control gate material of a predetermined thickness over the second dielectric, the thickness of the second dielectric being less than the thickness of the first spacer, and the thickness of the second dielectric together with the thickness of the control gate material being greater than the thickness of the first spacer;

forming a word line mask; and

etching the control gate material layer, the second dielectric layer, and the strip through the word line mask to form a word line in self-alignment with the

floating gate material and insulated from the substrate by the first and second dielectrics, and a floating gate insulated from the substrate by the first dielectric.

18. The method of claim 17 further comprising:

forming a second spacer having a thickness equal to the thickness of the first spacer on the second sidewall of the strip;

implanting the dopant into the semiconductor substrate aligned at least in part to the second spacer; and

removing the second spacer prior to the second dielectric forming step.

19. A method of forming a nonvolatile floating gate memory cell, comprising:

forming a first doped region disposed in the semiconductor substrate;

forming a second doped region disposed in the semiconductor substrate and spaced apart from the first doped region, a channel region being defined in the semiconductor substrate between the first and second doped regions;

forming a floating gate disposed over a first part of the channel region and insulated therefrom by a first dielectric, the first dielectric being a tunnel dielectric and the floating gate having a top and a sidewall; and

forming a control gate having first and second sections respectively disposed upon the top and the sidewall of the floating gate, the second section of the control gate being insulated from the sidewall of the floating gate by a second dielectric, disposed over a second part of the channel adjacent the first doped region, and insulated from the second part of the channel by the first dielectric and the second dielectric.

20. The method of claim 19 wherein the control gate forming step further comprises forming the second section of the control gate over at least part of the first doped region and insulated therefrom by the first dielectric and the second dielectric.